

10/035503

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12886

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10035503	FILING DATE 10/25/2001	CLASS 438	SUBCLASS 199	GAU 2812	EXAMINER LATTIN
**APPLICANTS: Iguchi Katsuji; Hsu Sheng; Ono Yoshi; Maa Jer-shen;					
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A CIP OF 09/649,382 08/28/2000 ABN					
** FOREIGN APPLICATIONS VERIFIED:					
PG-PUB <input type="checkbox"/>		DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no				ATTORNEY DOCKET NO	
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no				SLA0636	
Verified and Acknowledged Examiners's initials					
TITLE : Method of fabricating deep sub-micron CMOS source/drain with MDD and selective CVD silicide					

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg. Print Fig.
		Application Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	
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